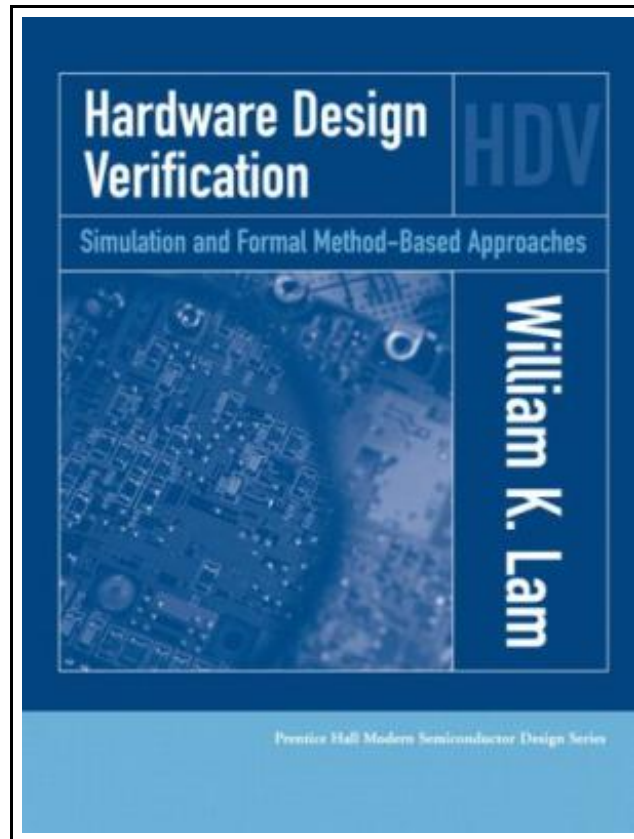# Hardware Design Verification: Simulation and Formal Method-Based Approaches (Paperback)

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Pearson Education (US), United States, 2008. Paperback. Book Condition: New. 234 x 176 mm. Language: English . Brand New Book. The Practical, Start-to-Finish Guide to Modern Digital Design Verification As digital logic designs grow larger and more complex, functional verification has become the number one bottleneck in the design process. Reducing verification time is crucial to project success, yet many practicing engineers have had little formal training in verification, and little exposure to the newest solutions. Hardware Design Verification systematically presents today s most valuable simulation-based and formal verification techniques, helping test and design engineers choose the best approach for each project, quickly gain confidence in their designs, and move into fabrication far more rapidly. College students will find that coverage of verification principles and common industry practices will help them prepare for jobs as future verification engineers. Author William K. Lam, one of the world s leading experts in design verification, is a recent winner of the Chairman s Award for Innovation, Sun Microsystems most prestigious technical achievement award. Drawing on his wide-ranging experience, he introduces the foundational principles of verification, presents traditional techniques that have survived the test of time, and introduces emerging techniques for today s most challenging designs. Throughout, Lam emphasizes practical examples rather than mathematical proofs; wherever advanced math is essential, he explains it clearly and accessibly. Coverage includes * Simulation-based versus formal verification: advantages, disadvantages, and tradeoffs* Coding for verification: functional and timing correctness, syntactical and structure checks, simulation performance, and more* Simulator architectures and operations, including event-driven, cycle-based, hybrid, and hardware-based simulators* Testbench organization, design, and tools: creating a fast, efficient test environment* Test scenarios and assertion: planning, test cases, test generators, commercial and Verilog assertions, and more* Ensuring complete coverage, including code, parameters, functions, items, and cross-coverage* The verification cycle: failure capture,...

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